

### 1. General Description

The WP5801 is a USB Type-C port protection chip that provides 20-V Short-to-VBUS overvoltage and IEC ESD protection.

By integrating low on-resistance power switch and low capacitance TVS, the WP5801 protects USB Type-C ports CC, SBU and D+/D- that undergoing overvoltage and IEC 61000-4-2 system level ESD without interfering with normal operation.

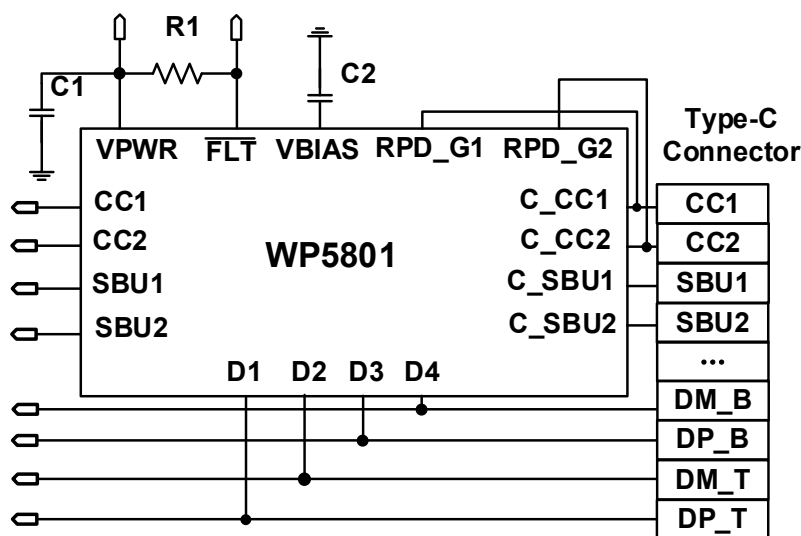
### 2. Features

- Short to VBUS Overvoltage Protection for CC1, CC2, SBU1 and SBU2
- IEC 61000-4-2 ESD Protection for CC1, CC2, SBU1, SBU2, DP\_T, DM\_T, DP\_B, DM\_B
- Low on-resistance protection FET for CC1 and CC2 passing 600 mA  $V_{CONN}$  current
- Fast OVP response for CCX and SBUX
- CC Dead Battery Resistors integrated for handling dead battery use case in mobile devices
- Package: 3-mm × 3-mm WQFN

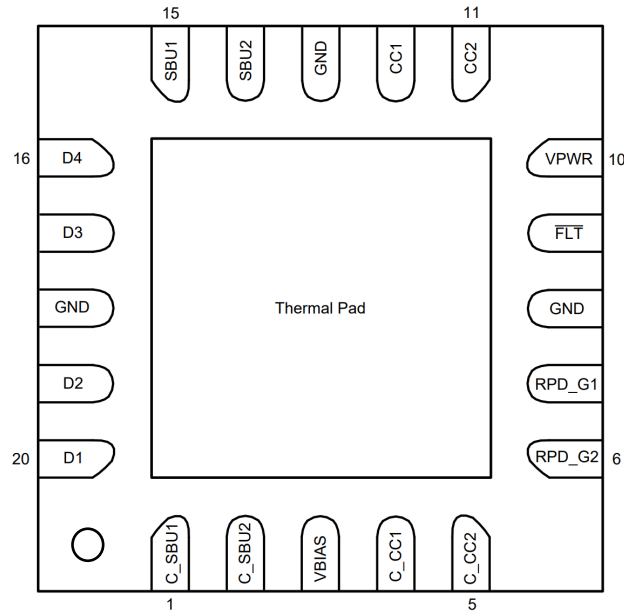
### 3. Applications

- Laptop PC
- Tablets
- Smart phones
- Monitors and TVS
- Docking Stations

### 4. Typical Application



## 5. Pin Configuration



TOP VIEW

## 6. Pin Description

PIN NUMBER	PIN NAME	I/O	PIN FUNCTIONS
1	C_SBU1	I/O	Connector side of the SBU1 OVP FET. Connect to either SBU pin of the USB Type-C connector.
2	C_SBU2	I/O	Connector side of the SBU2 OVP FET. Connect to either SBU pin of the USB Type-C connector.
3	VBIAS	Power	Pin for ESD support capacitor. Place a 0.1- $\mu$ F capacitor on this pin to ground.
4	C_CC1	I/O	Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector.
5	C_CC2	I/O	Connector side of the CC2 OVP FET. Connect to either CC pin of the USB Type-C connector.
6	RPD_G2	I/O	Short to C_CC2 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
7	RPD_G1	I/O	Short to C_CC1 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
8	GND	GND	Ground.
9	$\overline{\text{FLT}}$	O	Open drain for fault reporting. Under over temperature & over voltage conditions, pull low. Otherwise stay high-Z. Connect to VPWR by external resistor.

PIN NUMBER	PIN NAME	I/O	PIN FUNCTIONS
10	VPWR	Power	2.7V – 5.5V power supply.
11	CC2	I/O	System side of the CC2 OVP FET. Connect to either CC pin of the CC/PD controller.
12	CC1	I/O	System side of the CC1 OVP FET. Connect to either CC pin of the CC/PD controller.
13	GND	GND	Ground.
14	SBU2	I/O	System side of the SBU2 OVP FET. Connect to either SBU pin of the SBU MUX.
15	SBU1	I/O	System side of the SBU1 OVP FET. Connect to either SBU pin of the SBU MUX.
16	D4	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector.
17	D3	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector.
18	GND	GND	Ground.
19	D2	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector.
20	D1	I/O	USB2.0 IEC ESD protection. Connect to any of the USB2.0 pins of the USB Type-C connector.
-	Thermal Pad	GND	Internally connected to GND. Used as a heatsink. Connect to the PCB GND plane.

## 7. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>[1]</sup>

	PARAMETER	RATING	UNIT
Input Voltage	VPWR	-0.3 to 6	V
	RPD_G1, RPD_G2	-0.3 to 24	V
Output Voltage	$\overline{\text{FLT}}$	-0.3 to 6	V
	VBIAS	-0.3 to 24	V
I/O Voltage	D1, D2, D3, D4	-0.3 to 6	V
	CC1, CC2, SBU1, SBU2	-0.3 to 6	V
	C_CC1, C_CC2, C_SBU1, C_SBU2	-0.3 to 24	V
Operating Free Air Temperature		-40 to 85	°C
Storage Temperature		-65 to 150	°C

**NOTE [1]:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 8. ESD Ratings—JEDEC Specification

PARAMETER		VALUE	UNIT
Electrostatic Discharge	Human-Body Model (HBM), Per ANSI/ESDA/JEDEC JS-001 <sup>[2]</sup>	±4000	V

**NOTE [2]:** JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

## 9. ESD Ratings—IEC Specification

PARAMETER		VALUE	UNIT
Electrostatic Discharge	IEC 61000-4-2, D1, D2, D3, D4	Contact Discharge	±8000
		Air-gap Discharge	±15000
	IEC 61000-4-2, C_SBU1, C_SBU2	Contact Discharge	±6000
		Air-gap Discharge	±15000
	IEC 61000-4-2, C_CC1, C_CC2	Contact Discharge	±3500
		Air-gap Discharge	±15000

## 10. Recommended Operating Conditions

(Over operating free-air temperature range, unless otherwise noted)

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V <sub>IN</sub>	Input Voltage	VPWR	2.7	3.3	5.5	V
		RPD_G1, RPD_G2	0		5.5	V
V <sub>OUT</sub>	FLT Pull-up Resistor Power Rail		2.7		5.5	V
V <sub>IO</sub>	I/O Voltage	D1, D2, D3, D4	-0.3		5.5	V
		CC1, CC2, C_CC1, C_CC2	0		5.5	V
		SBU1, SBU2, C_SBU1, C_SBU2	0		4.3	V
I <sub>VCONN</sub>	V <sub>CONN</sub> Current	Current flowing into CC1/2 and flowing out of C_CC1/2, V <sub>CCX</sub> - V <sub>C_CCX</sub> ≤ 250 mV			600	mA
I <sub>VCONN</sub>	V <sub>CONN</sub> Current	Current flowing into CC1/2 and flowing out of C_CC1/2, T <sub>J</sub> ≤ 105°C			1.25	A
	External Components <sup>[3]</sup>	FLT Pull-up Resistance	1.7		300	kΩ
		VBIAS Capacitance <sup>[4]</sup>		0.1		μF
		VPWR Capacitance	0.3	1		μF

**NOTE [3]:** For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented must be within the minimum and maximums listed in the table.

**NOTE [4]:** The VBIAS pin requires a minimum 35-V<sub>DC</sub> rated capacitor. A 50-V<sub>DC</sub> rated capacitor is recommended to reduce capacitance derating. See the VBIAS Capacitor Selection section for more information on selecting the VBIAS capacitor.

## 11. Electrical Characteristics

(Over operating free-air temperature range, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
<b>CC OVP Switches</b>						
$R_{ON}$	On resistance of CC OVP FETs, $T_J \leq 85^\circ\text{C}$	$CCX = 5.5\text{ V}$		300	600	$\text{m}\Omega$
$R_{ONFLAT}$	On resistance flatness	Sweep CCX voltage between 0V and 1.2V			5	$\text{m}\Omega$
$C_{ON\_CC}$	Equivalent on capacitance	Capacitance from C_CCX or CCX to GND. $V_{C\_CCX/VCCX} = 0\text{ V to }1.2\text{ V}$ , $f = 400\text{ kHz}$	30	74	90	$\text{pF}$
$R_{D\_DB}$	Dead battery pull-down resistance (only present when device is unpowered). Effective resistance of RD and FET in series	$V_{C\_CCX} = 2.6\text{ V}$	4.1	5.1	6.1	$\text{K}\Omega$
$V_{TH\_DB}$	Threshold voltage of the pulldown FET in series with RD during dead battery	$I_{CC} = 80\ \mu\text{A}$	0.5	0.9	1.2	V
$V_{OVCC}$	OVP threshold on CC pins	Place 5.5 V on C_CCX. Step up C_CCX until the $\overline{\text{FLT}}$ pin is asserted	5.75	6	6.2	V
$V_{OVCC\_HYS}$	Hysteresis on CC OVP	Place 6.5 V on C_CCX. Step down the voltage on C_CCX until the $\overline{\text{FLT}}$ pin is deasserted. Measure difference between rising and falling OVP threshold for CC		50		$\text{mV}$
$BW_{ON}$	On bandwidth single ended (-3 dB)	Measure the -3-dB bandwidth from C_CCX to CCX. Single ended measurement, 50 $\Omega$ system $V_{CM} = 0.1\text{ V to }1.2\text{ V}$		100		$\text{MHz}$
$V_{STBUS\_CC}$	Short-to-VBUS tolerance on the CC pins	Hot-Plug C_CCX with a 1meter USB Type C Cable, place a 30- $\Omega$ load on CCX			24	V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>STBUS_CC_CLAMP</sub>	Short-to-VBUS system-side clamping voltage on the CC pins (CCX)	Hot-Plug C <sub>CCX</sub> with a 1-meter USB Type C Cable. Hot-Plug voltage C <sub>CCX</sub> = 24 V. VPWR = 3.3 V. Place a 30Ω load on CCX		6		V
<b>SBU OVP Switches</b>						
R <sub>ON</sub>	On resistance of SBU OVP FETs	SBUX = 3.6 V, -40°C ≤ T <sub>J</sub> ≤ +85°C		3.5	6.5	Ω
R <sub>ONFLAT</sub>	On resistance flatness	Sweep SBUX voltage between 0 V and 3.6 V. -40°C ≤ T <sub>J</sub> ≤ +85°C		1	1.5	Ω
C <sub>ON_SBU</sub>	Equivalent on capacitance	Capacitance from SBUX or C <sub>SBUX</sub> to GND. Measure at V <sub>C_SBUX</sub> /V <sub>SBUX</sub> = 0.3 V to 3.6 V		9		pF
V <sub>OVPSBU</sub>	OVP threshold on SBU pins	Place 3.6 V on C <sub>SBUX</sub> . Step up C <sub>SBUX</sub> until the $\overline{\text{FLT}}$ pin is asserted	4.3	4.5	4.75	V
V <sub>OVPSBU_HYS</sub>	Hysteresis on SBU OVP	Place 5 V on C <sub>CCX</sub> . Step down the voltage on C <sub>CCX</sub> until the $\overline{\text{FLT}}$ pin is deasserted. Measure difference between rising and falling OVP threshold for C <sub>SBUX</sub>		60		mV
BW <sub>ON</sub>	On bandwidth single ended (-3 dB)	Measure the -3-dB bandwidth from C <sub>SBUX</sub> to SBUX. Single ended measurement, 50-Ω system. V <sub>CM</sub> = 0.1 V to 3.6 V		1000		MHz
X <sub>TALK</sub>	Crosstalk	Measure crosstalk at f = 1 MHz from SBU1 to C <sub>SBU2</sub> or SBU2 to C <sub>SBU1</sub> . V <sub>CM1</sub> = 3.6 V, V <sub>CM2</sub> = 0.3V. Be sure to terminate open sides to 50 Ω		-80		dB
V <sub>STBUS_SBU</sub>	Short-to-VBUS tolerance on the SBU pins	Hot-Plug C <sub>SBUX</sub> with a 1-meter USB Type C Cable. Put a 40Ω resistor to GND on SBUX			24	V



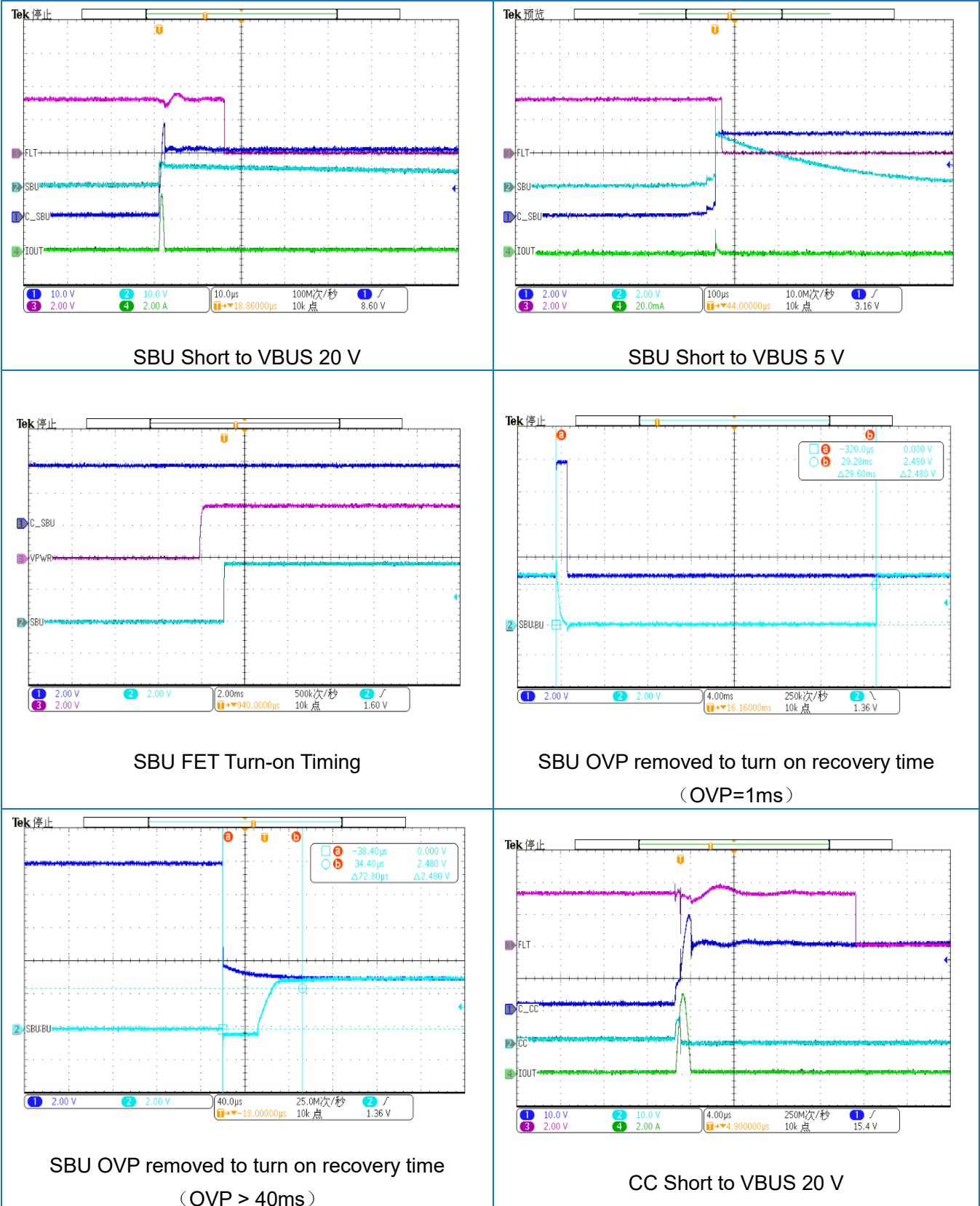
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>STBUS_SBU_C</sub> LAMP	Short-to-VBUS system-side clamping voltage on the SBU pins (SBUX)	Hot-Plug C_SBUX with a 1-meter USB Type C Cable. Hot-Plug voltage V <sub>C_SBUX</sub> = 24 V. V <sub>PWR</sub> = 3.3 V. Put a 40Ω resistor to GND on SBUX		4.5		V
<b>Power Supply and Leakage Currents</b>						
V <sub>PWR_UVLO</sub>	VPWR under voltage lockout	Place 1 V on VPWR and raise voltage until SBU or CC FETs turn on	2.1	2.3	2.5	V
V <sub>PWR_UVLO</sub> _HYS	VPWR UVLO hysteresis	Place 3 V on VPWR and lower voltage until SBU or CC FETs turnoff; measure difference between rising and falling UVLO to calculate hysteresis		100		mV
I <sub>VPWR</sub>	VPWR supply current	V <sub>PWR</sub> = 3.3 V (Typical), -40°C ≤ T <sub>J</sub> ≤ +85°C.		70	120	μA
I <sub>CC_LEAK</sub>	Leakage current for CC pins when device is powered	V <sub>PWR</sub> = 3.3 V, V <sub>C_CCX</sub> = 3.6 V, CCX pins are floating, measure leakage into C_CCX pins. Result must be same if CCX side is biased and C_CCX is left floating.			5	μA
I <sub>SBU_LEAK</sub>	Leakage current for SBU pins when device is powered	V <sub>PWR</sub> = 3.3 V, V <sub>C_SBUX</sub> = 3.6V, SBUX pins are floating, measure leakage into C_SBUX pins. Result must be same if SBUX side is biased and C_SBUX is left floating. -40°C ≤ T <sub>J</sub> ≤ 85°C.			3	μA
I <sub>C_CC_LEAK</sub> _OVP	Leakage current for CC pins when device is in OVP	V <sub>PWR</sub> = 0 V or 3.3 V, V <sub>C_CCX</sub> = 24V, CCX pins are set to 0 V, Measure leakage into C_CCX pins			200	μA

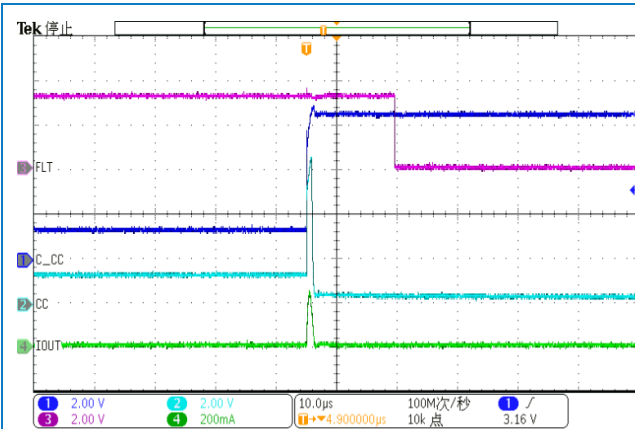
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
$I_{C\_SBU\_LEAK\_OVP}$	Leakage current for SBU pins when device is in OVP	$V_{PWR} = 0\text{ V or }3.3\text{ V}$ , $V_{C\_SBUX} = 24\text{ V}$ , SBUX pins are set to 0 V, measure leakage into C_SBUX pins			200	$\mu\text{A}$
$I_{CC\_LEAK\_OVP}$	Leakage current for CC pins when device is in OVP	$V_{PWR} = 0\text{ V or }3.3\text{ V}$ , $V_{C\_CCX} = 24\text{ V}$ , CCX pins are set to 0 V, measure leakage out of CCX pins			30	$\mu\text{A}$
$I_{SBU\_LEAK\_OVP}$	Leakage current for SBU pins when device is in OVP	$V_{PWR} = 0\text{ V or }3.3\text{ V}$ , $V_{C\_SBUX} = 24\text{ V}$ , SBUX pins are set to 0 V, measure leakage out of SBUX pins	-1		1	$\mu\text{A}$
$I_{DX\_LEAK}$	Leakage current for Dx pins	$V_{DX} = 3.6\text{ V}$ , measure leakage into Dx pins			1	$\mu\text{A}$
<b><math>\overline{\text{FLT}}</math> Pin</b>						
$V_{OL}$	Low-level output voltage	$I_{OL} = 3\text{ mA}$ . Measure the voltage at the FLT pin			0.4	V
<b>Over Temperature Protection</b>						
$T_{SD\_RISING}$	The rising over-temperature protection shutdown threshold			170		$^{\circ}\text{C}$
$T_{SD\_FALLING}$	The falling over-temperature protection shutdown threshold			135		$^{\circ}\text{C}$
$T_{SD\_HYST}$	The over-temperature protection shutdown threshold hysteresis			35		$^{\circ}\text{C}$
<b>Dx ESD Protection</b>						
$V_{RWM\_POS}$	Reverse stand-off voltage from Dx to GND	Dx to GND. $IDX \leq 1\ \mu\text{A}$			5.5	V
$V_{RWM\_NEG}$	Reverse stand-off voltage from GND to Dx	GND to Dx			0	V
$V_{BR\_POS}$	Break-down voltage from Dx to GND	Dx to GND. $IBR = 1\text{ mA}$	7			V
$V_{BR\_NEG}$	Break-down voltage from GND to Dx	GND to Dx. $IBR = 8\text{ mA}$	0.6			V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
$C_{IO}$	Capacitance Dx to GND or GND to Dx	$f = 1 \text{ MHz}, V_{IO} = 2.5 \text{ V}$		2.5		pF
$\Delta C_{IO}$	Differential capacitance between two Dx pins	$f = 1 \text{ MHz}, V_{IO} = 2.5 \text{ V}$		1		pF
$R_{DYN}$	Dynamic on-resistance Dx IEC clamps	Dx to GND or GND to Dx		0.4		$\Omega$
<b>Power-On and Off Timings</b>						
$t_{ON}$	Time from crossing rising VPWR UVLO until CC and SBU OVP FETs are on				3.5	ms
$d_{VPWR\_OFF/dt}$	Minimum slew rate allowed to guarantee CC and SBU FETs turnoff during a power off		-0.5			V/ $\mu$ s
<b>Over Voltage Protection</b>						
$t_{OVP\_RESPONS\_E\_CC}$	OVP response time on the CC pins. Time from OVP asserted until OVP FETs turnoff			80		ns
$t_{OVP\_RESPONS\_E\_SBU}$	OVP response time on the SBU pins. Time from OVP asserted until OVP FETs turnoff			130		ns
$t_{OVP\_RECOVER\_Y\_CC\_1}$	OVP recovery time on the CC pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on. OVP must be removed for CC FETs to turn back on		21	33	39	ms
$t_{OVP\_RECOVER\_Y\_SBU\_1}$	OVP recovery time on the SBU pins. Once an OVP has occurred, the minimum time duration until the SBU FETs turn back on. OVP must be removed for SBU FETs to turn back on		21	32	39	ms
$t_{OVP\_RECOVER\_Y\_CC\_2}$	OVP recovery time on the CC pins. Time from OVP removal until CC FET turns back on, if device has been in OVP > 40 ms			0.1		ms
$t_{OVP\_RECOVER\_Y\_SBU\_2}$	OVP recovery time on the SBU pins. Time from OVP removal until SBU FET turns back on, if device has been in OVP > 40 ms			0.1		ms
$t_{OVP\_FLT\_ASSERTION}$	Time from OVP asserted to $\overline{FLT}$ assertion			12		$\mu$ s
$t_{OVP\_FLT\_DEASSERTION}$	Time from CC FET turn on after an OVP to $\overline{FLT}$ Deassertion			5		ms

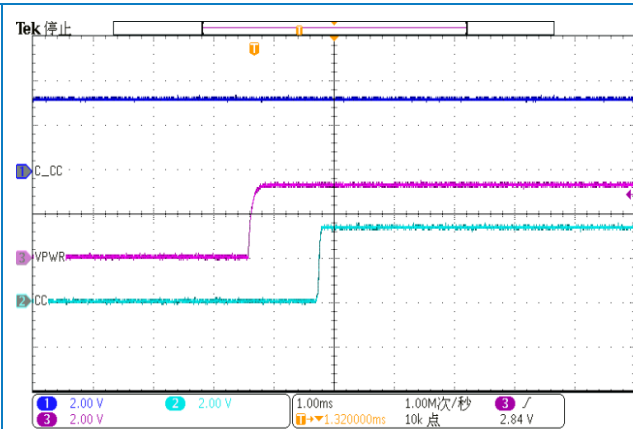
## 12. Typical Performance Characteristics

( $V_{PWR} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $C_1 = 1\mu F$ ,  $C_2 = 0.1\mu F$ ,  $R_1 = 100k\Omega$ , unless otherwise noted)

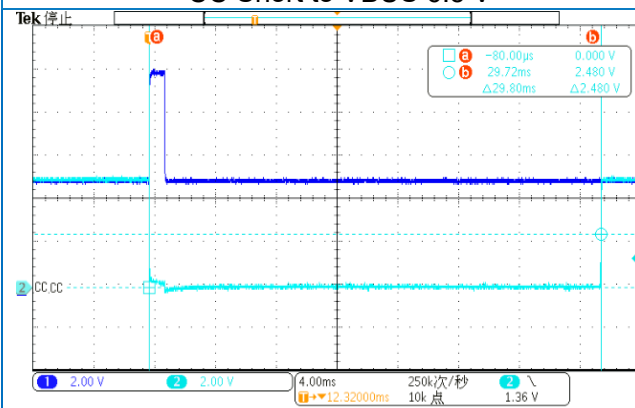




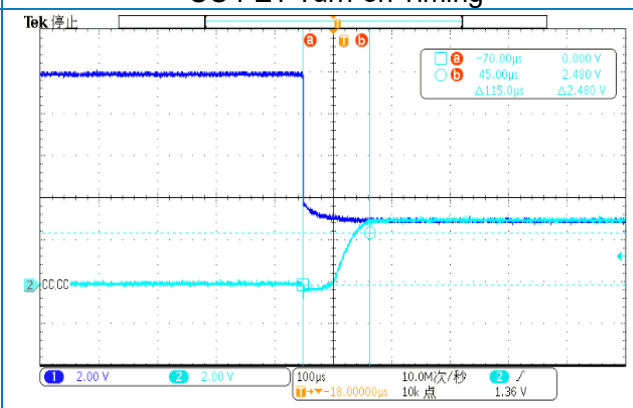
CC Short to VBUS 6.5 V



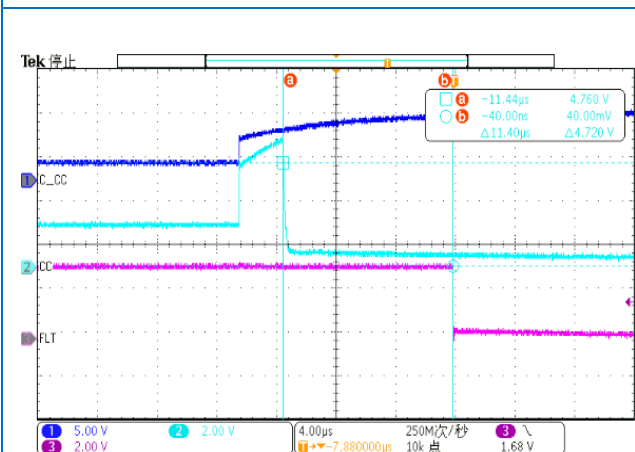
CC FET Turn-on Timing



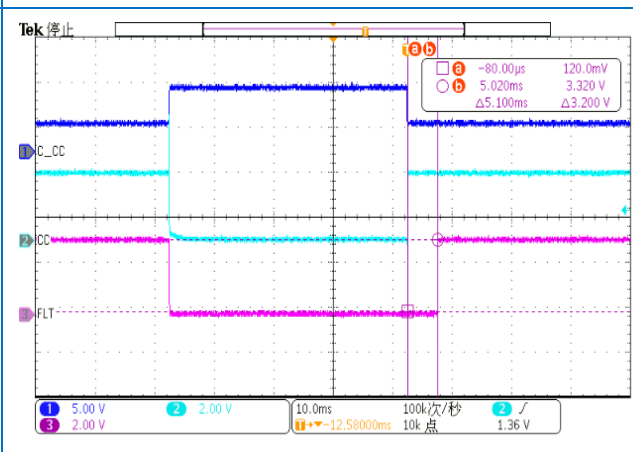
CC OVP removed to turn on recovery time  
(OVP = 1ms)



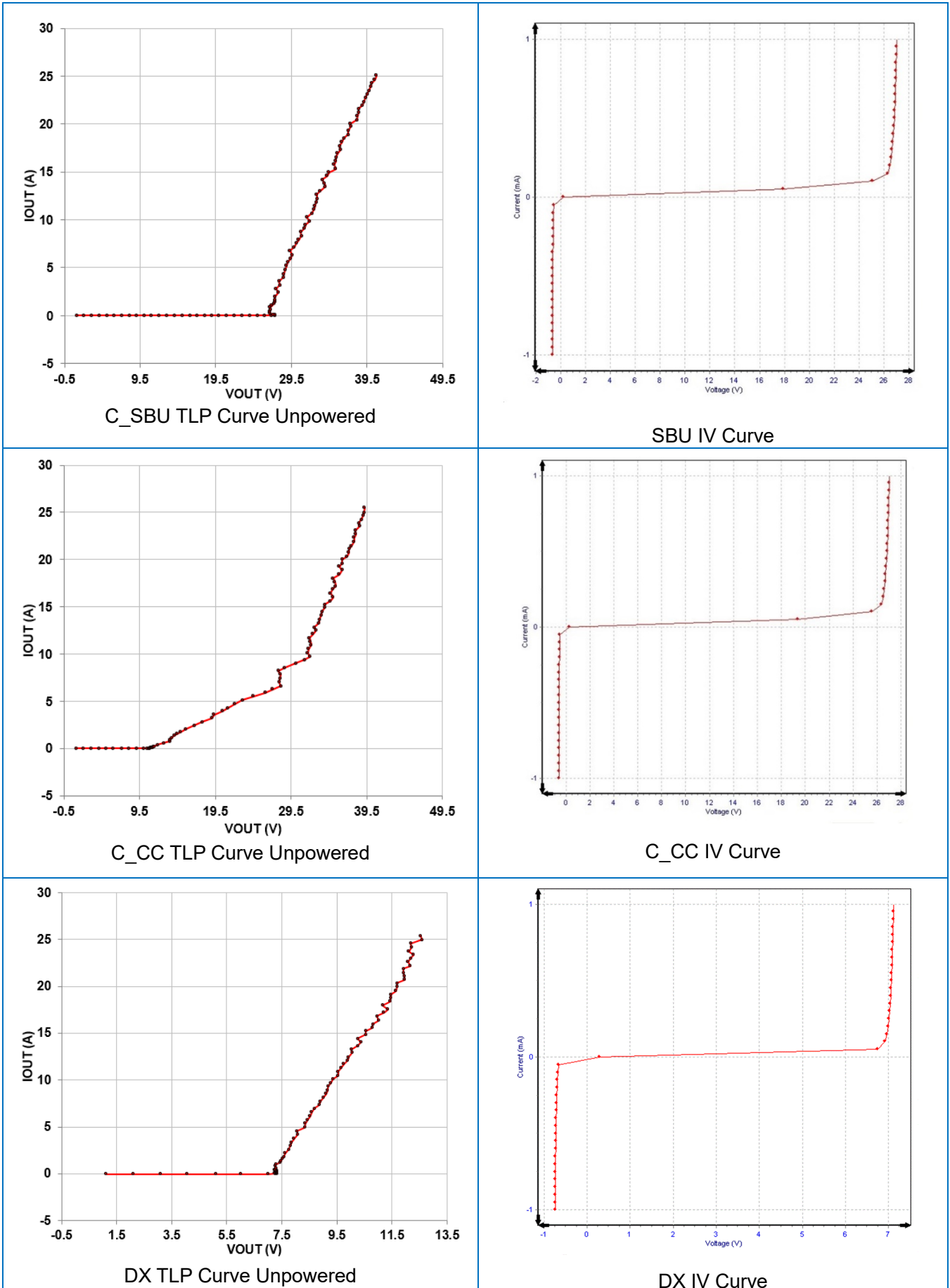
CC OVP removed to turn on recovery time  
(OVP > 40 ms)

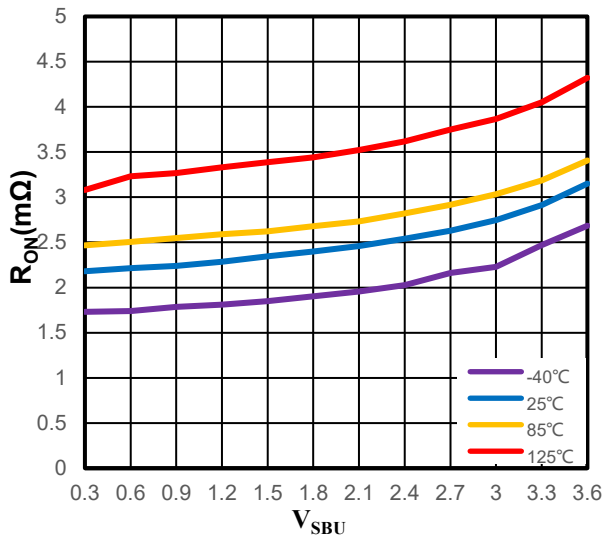


Time from OVP asserted to FLT assertion

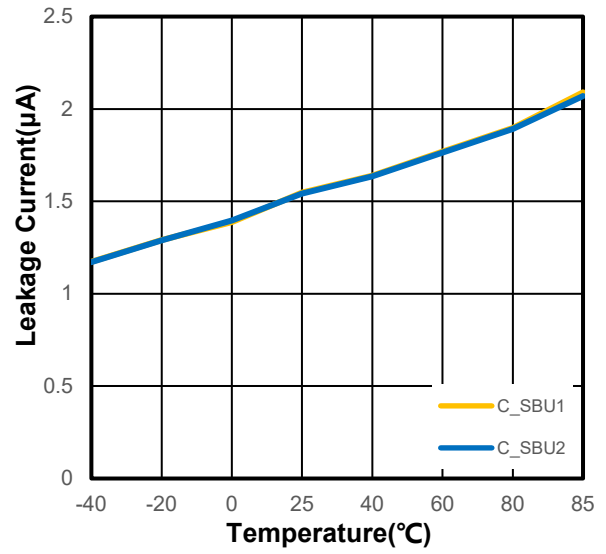


Time from CC FET turn on after an OVP to  $\overline{FLT}$   
deassertion

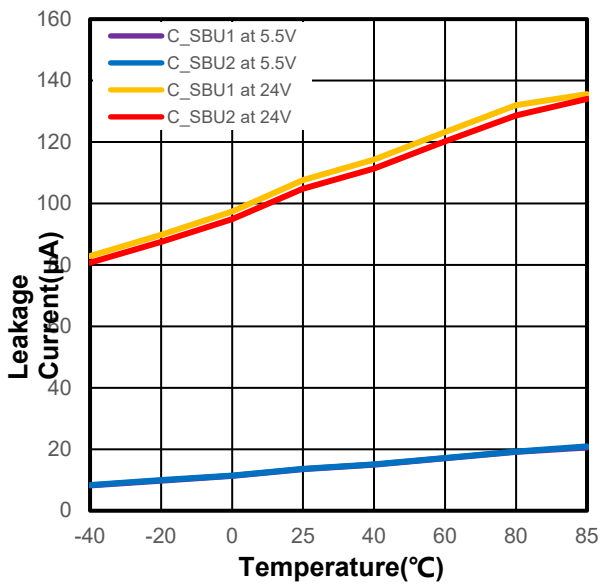




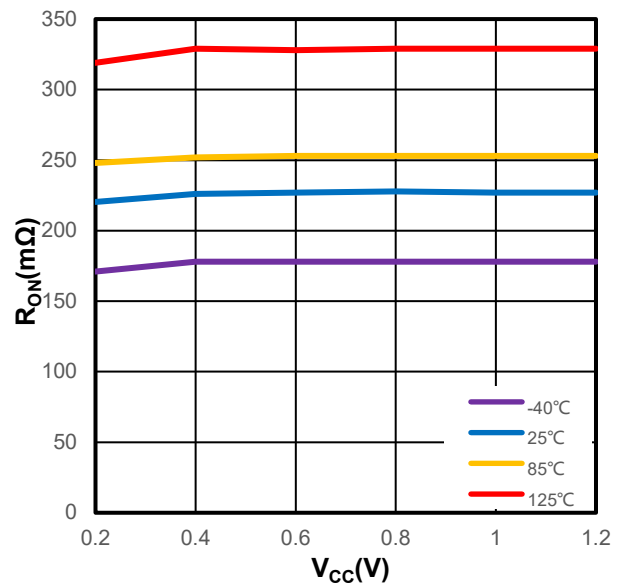
SBU RON Flatness



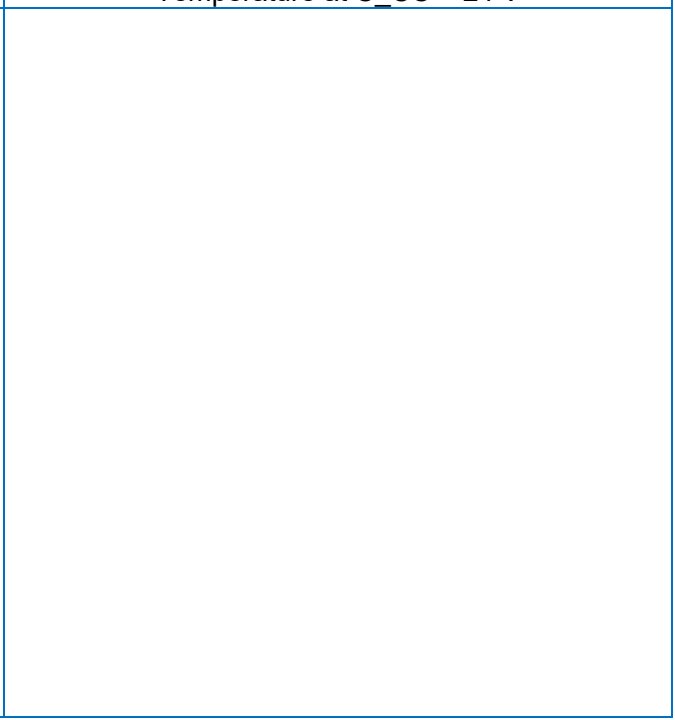
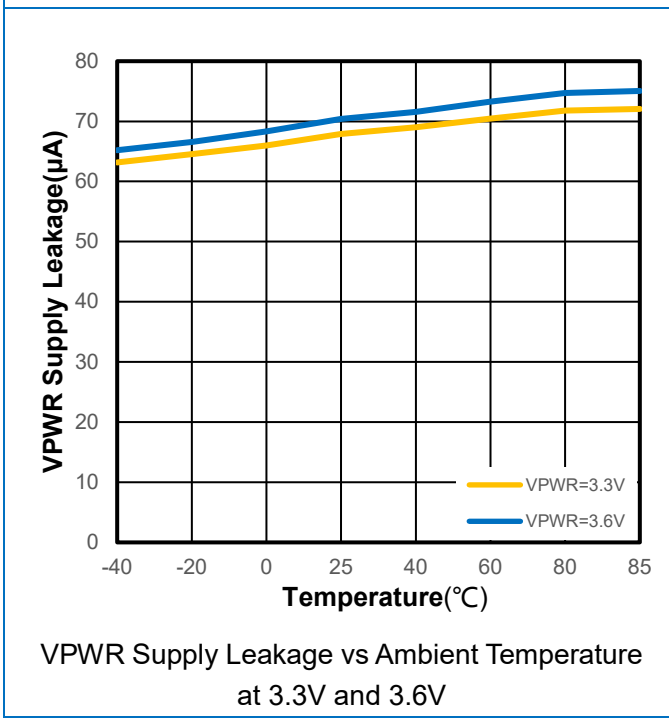
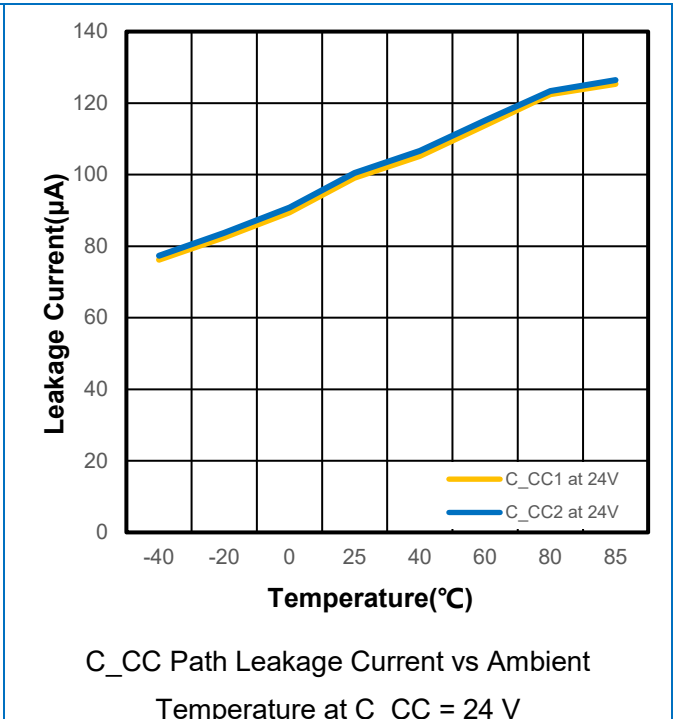
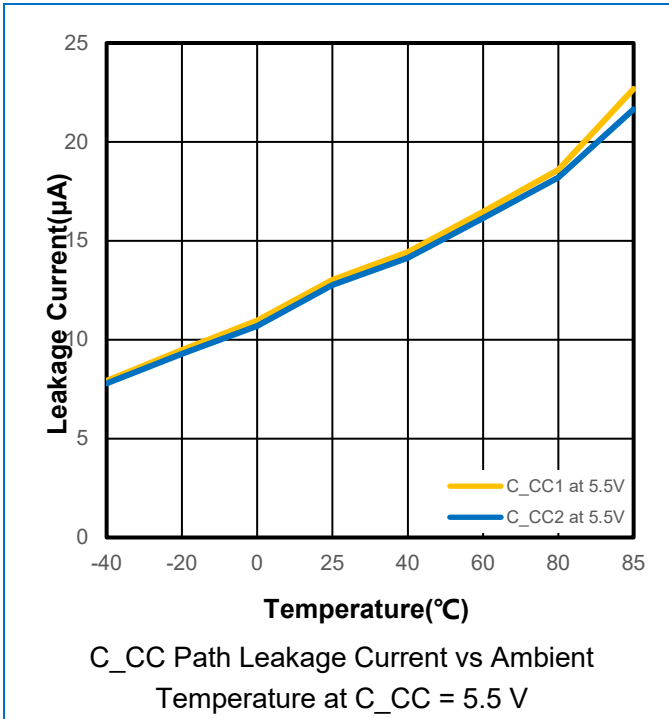
SBU Path Leakage Current vs Ambient Temperature at 3.6 V



C\_SBU OVP Leakage Current vs Ambient Temperature at 5.5 V and 24 V



CC RON Flatness



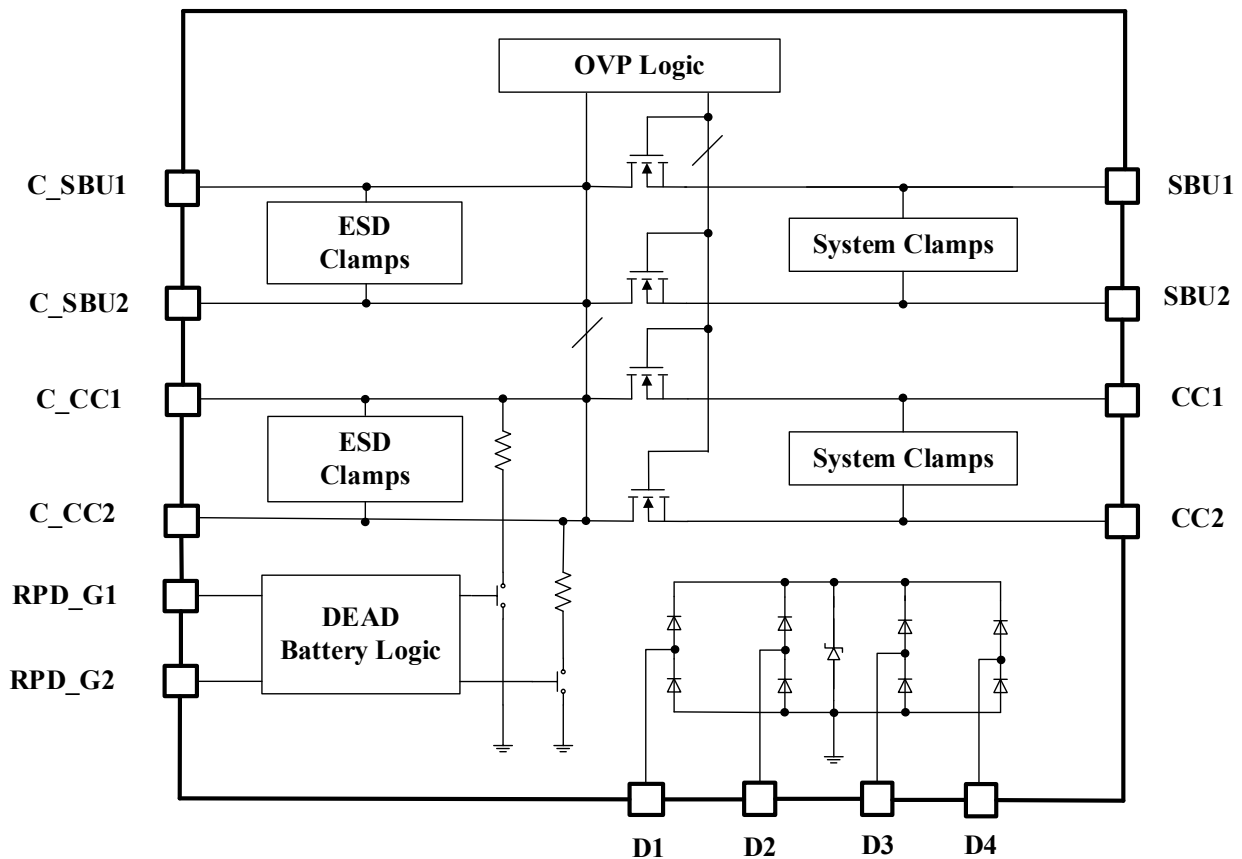


## 13. Function Description

### 13.1 Overview

The WP5801 is a USB Type-C port protection chip that integrates four channels of 20-V Short-to-VBUS overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins and eight channels of IEC61000-4-2 ESD protection for the CC1, CC2, SBU1, SBU2, DP\_T (Top side D+), DM\_T (Top Side D-), DP\_B (Bottom Side D+) and DM\_B (Bottom Side D-) pins of the USB Type-C connector.

### 13.2 Block Diagram



### 13.3 Feature Description

#### 13.3.1 4-Channels of Short-to-VBUS Overvoltage Protection (CC1, CC2, SBU1, SBU2 Pins): 24-V<sub>Dc</sub> Tolerant

The WP5801 provides 4-channels of Short-to-VBUS Overvoltage Protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector. The WP5801 is able to handle 24-V<sub>Dc</sub> on its C\_CC1, C\_CC2, C\_SBU1, and C\_SBU2 pins. This is necessary because according to the USB PD specification, with VBUS set for 20-V operation, the VBUS voltage is allowed to legally swing up to 21 V, and 21.5 V on voltage transitions from a different USB PD VBUS voltage.

**13.3.2 8-Channels of IEC 61000-4-2 ESD Protection (CC1, CC2, SBU1, SBU2, DP\_T, DM\_T, DP\_B, DM\_B Pins)**

The WP5801 integrates 8-Channels of IEC 61000-4-2 system level ESD protection for the CC1, CC2, SBU1, SBU2, DP\_T (Top side D+), DM\_T (Top Side D-), DP\_B (Bottom Side D+), and DM\_B (Bottom Side D-) pins. USB Type-C ports on end-products need system level IEC ESD protection in order to provide adequate protection for the ESD events that the connector can be exposed to from end users.

**13.3.3 Thermal Shutdown**

Thermal shutdown protects the part from internally or externally generated excessive temperatures. During an over temperature condition the switch is turned off. The switch automatically turns on again if the temperature of the die drops below the threshold temperature.

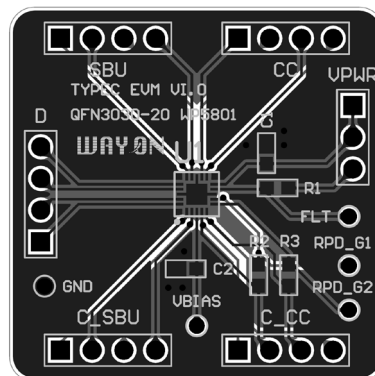
**13.3.4 Dead-battery Mode**

The WP5801 integrates high voltage dead battery RD pull-down resistors to allow dead battery charging simultaneously with high-voltage OVP protection. If dead battery support is required, short the RPD\_G1 pin to the C\_CC1 pin, and short the RPD\_G2 pin to the C\_CC2 pin. This connects the dead battery resistors to the connector CC pins.

**14. Layout**

For best performance, place the bypass capacitors as close as possible to the VPWR pin, and ESD protection capacitor as close as possible to the VBIAS pin. The USB2.0 and SBU lines must be routed as straight as possible and any sharp bends must be minimized.

**14.1 Layout Example**



## 15. Evaluation Modules

---

Evaluation Modules (EVMs) are available to help evaluate initial circuit performance. We have evaluation modules for different packages, you can contact us by phone or address at the end to get the evaluation module or schematic.

The module names are listed in the table below.

NAME	PACKAGE	EVALUATION MODULE
WP5801	QFN20 3*3	TYPEC EVM V1.0 QFN3030-20 WP5801

## 16. Naming Conventions

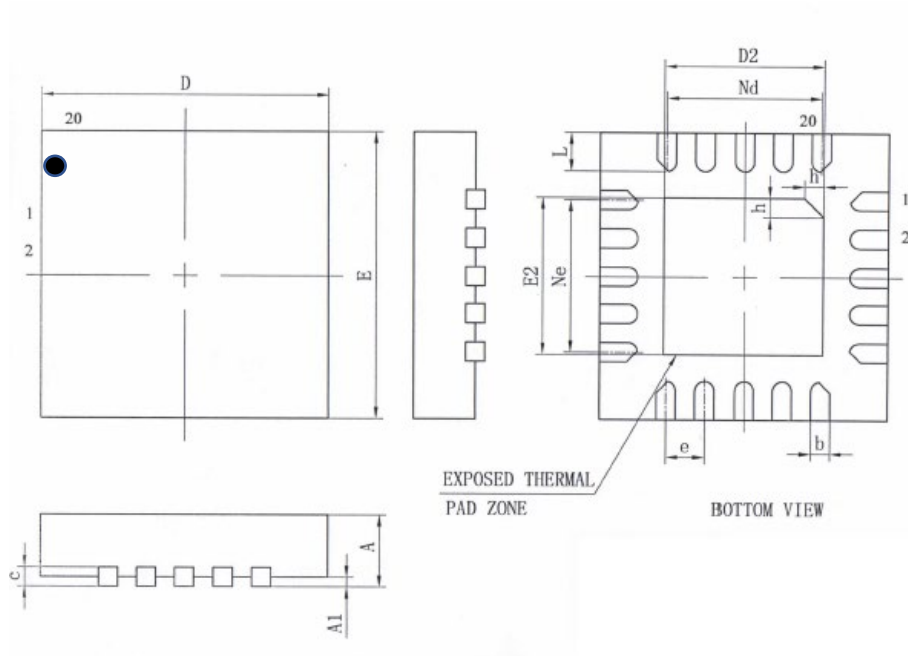
---

### WP AB CC-DDD E

- WP:** WAYON Protection IC;
- A:** Product Category –5: Type C Protection;
- B:** Number of Protection Channels –8: 8 Channels;
- CC:** Serial Number;
- DDD:** Package – Q3G: WQFN3\*3-20L;
- E:** R-Reel & T-tube;

## 17. Package Information

### QFN20 3\*3



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
<b>A</b>	0.7	0.75	0.8
<b>A1</b>	-	0.02	0.05
<b>b</b>	0.15	0.20	0.25
<b>c</b>	0.18	0.20	0.25
<b>D</b>	2.90	3.00	3.10
<b>D2</b>	1.55	1.65	1.75
<b>e</b>	0.40BSC		
<b>Ne</b>	1.60 BSC		
<b>ND</b>	1.60 BSC		
<b>E</b>	2.90	3.00	3.10
<b>E2</b>	1.55	1.65	1.75
<b>L</b>	0.35	0.40	0.45
<b>h</b>	0.20	0.25	0.30
<b>L/F MIL</b>	75*75		

## 18. Ordering Information

---

PART NUMBER	PACKAGE	PACKING QUANTITY	MARKING*
WP5801-Q3GR	QFN3*3-20L	3k/Reel	WP5801 XXXX

\* XXXX is variable.

### **STATEMENTS**

WAY-ON provides data sheets based on the actual performance of the device, and users should verify actual device performance in their specific applications. The device characteristics and parameters in this data sheet can and do vary from application to application, and actual device performance may change over time. This information is intended for developers designing with WAY-ON products. Users are responsible for selecting the appropriate WAY-ON product for their application and for designing and verifying the application to ensure that your application meets the appropriate standards or other requirements, and users are responsible for all consequences. Specifications are subject to change without notice.

### **Contact Information**

No.1001, Shiwan(7) Road, Pudong District, Shanghai, P.R.China.201202

Tel: 86-21-68960674 Fax: 86-21-50757680 Email: [market@way-on.com](mailto:market@way-on.com)

WAYON website: <http://www.way-on.com>

For additional information, please contact your local Sales Representative.

**WAYON**® is registered trademark of Wayon Corporation.

*Specifications are subject to change without notice.*

*The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.*

*Users should verify actual device performance in their specific applications.*