

## 60V Dual N-Channel Enhancement Mode Power MOSFET

### Description

WMB03DN06T1 uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Features

- $V_{DS} = 60V$ ,  $I_D = 6A$   
 $R_{DS(on)} < 110m\Omega @ V_{GS} = 10V$   
 $R_{DS(on)} < 120m\Omega @ V_{GS} = 4.5V$
- Low Gate Charge
- 100% EAS Guaranteed

### Applications

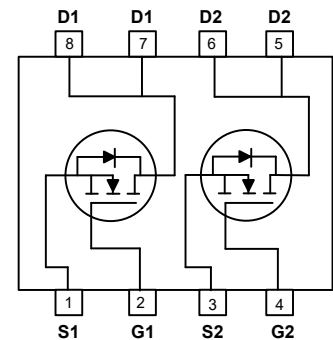
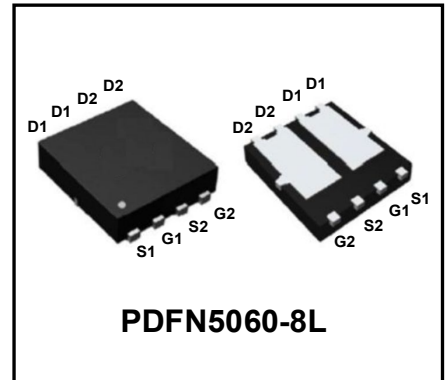
- Power Management in Switches
- DC/DC Converter

### Absolute Maximum Ratings ( $T_A = 25^\circ C$ , unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_C = 25^\circ C$	$I_D$	6	A
	$T_C = 100^\circ C$		3.8	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	24	A
Single Pulse Avalanche Energy <sup>2</sup>		<b>EAS</b>	7.9	mJ
Total Power Dissipation	$T_C = 25^\circ C$	$P_D$	6.94	W
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	60	$^\circ C/W$
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	18	$^\circ C/W$



**Electrical Characteristics** ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60	-	-	V
Gate-body Leakage Current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$T_J=25^\circ\text{C}$	$V_{DS} = 60V, V_{GS} = 0V$	-	-	1	$\mu A$
	$T_J=100^\circ\text{C}$		-	-	100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.8	1.3	2	V
Drain-Source On-Resistance <sup>4</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 3A$	-	80	110	m $\Omega$
		$V_{GS} = 4.5V, I_D = 2A$	-	90	120	
Forward Transconductance <sup>4</sup>	$g_{fs}$	$V_{GS} = 10V, I_D = 3A$	-	7	-	S
<b>Dynamic Characteristics<sup>5</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 30V, V_{GS} = 0V, f = 1\text{MHz}$	-	530	-	pF
Output Capacitance	$C_{oss}$		-	24	-	
Reverse Transfer Capacitance	$C_{rss}$		-	20	-	
Gate Resistance	$R_g$	$f = 1\text{MHz}$	-	2.2	-	$\Omega$
<b>Switching Characteristics<sup>5</sup></b>						
Total Gate Charge	$Q_g$	$V_{GS} = 10V, V_{DS} = 30V, I_D = 3A$	-	5	-	nC
Gate-Source Charge	$Q_{gs}$		-	1.7	-	
Gate-Drain Charge	$Q_{gd}$		-	1.5	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 30V, R_G = 3\Omega, I_D = 3A$	-	6	-	ns
Rise Time	$t_r$		-	14.5	-	
Turn-Off Delay Time	$t_{d(off)}$		-	15	-	
Fall Time	$t_f$		-	9.8	-	
<b>Drain-Source Body Diode Characteristics</b>						
Diode Forward Voltage <sup>4</sup>	$V_{SD}$	$I_S = 3A, V_{GS} = 0V$	-	-	1.2	V
Continuous Source Current	$T_C=25^\circ\text{C}$	$I_S$	-	-	6	A

## Notes:

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ .
2. The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.4\text{mH}, I_{AS}=6.3A$ .
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
5. This value is guaranteed by design hence it is not included in the production test.

### Typical Characteristics

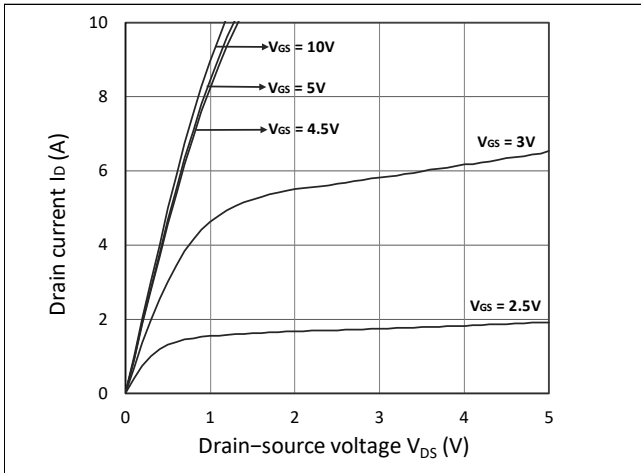


Figure 1. Output Characteristics

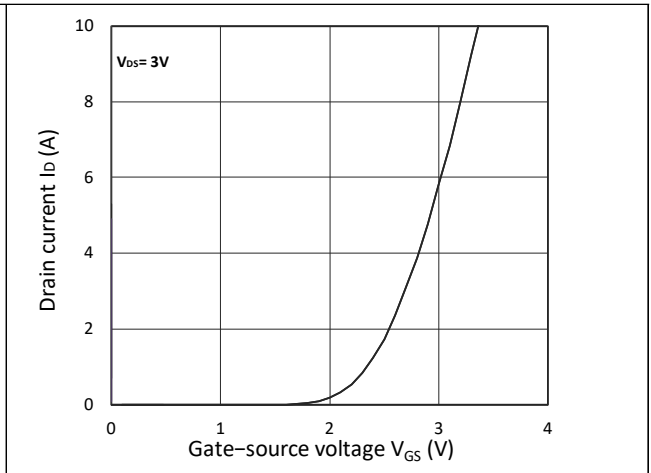


Figure 2. Transfer Characteristics

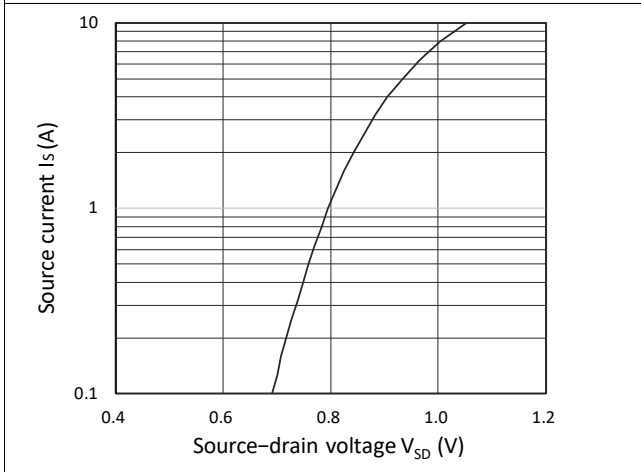


Figure 3. Forward Characteristics of Reverse

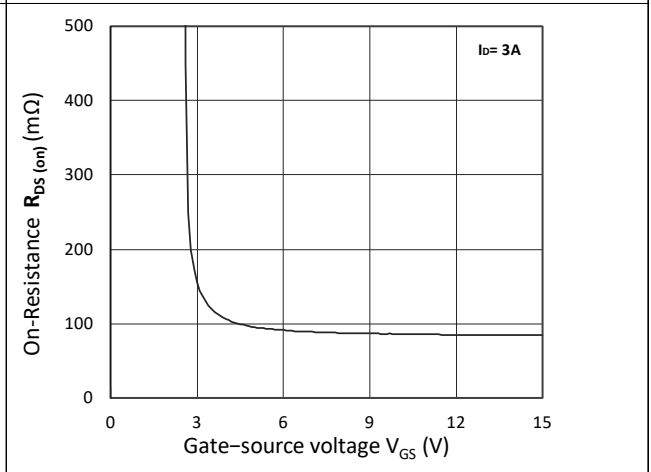


Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$

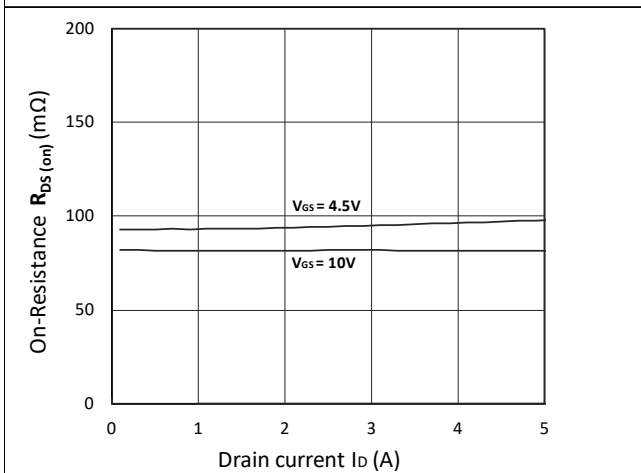


Figure 5.  $R_{DS(ON)}$  vs.  $I_D$

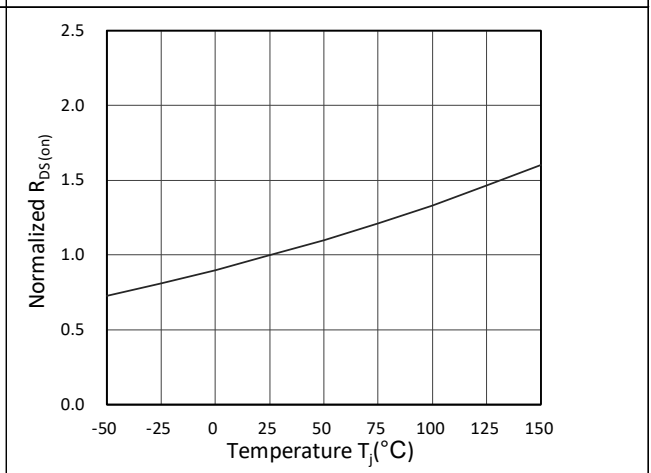


Figure 6. Normalized  $R_{DS(ON)}$  vs. Temperature

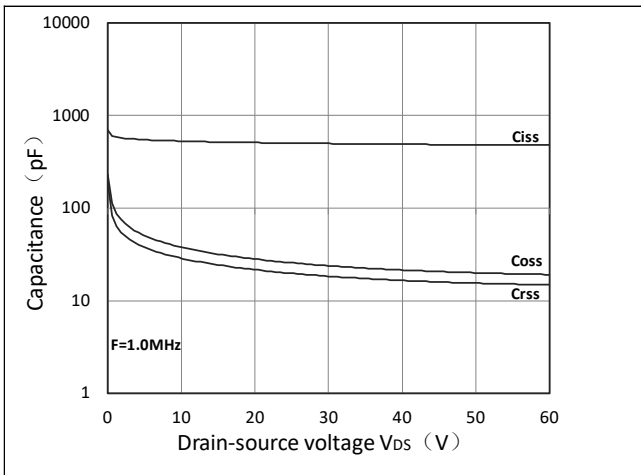


Figure 7. Capacitance Characteristics

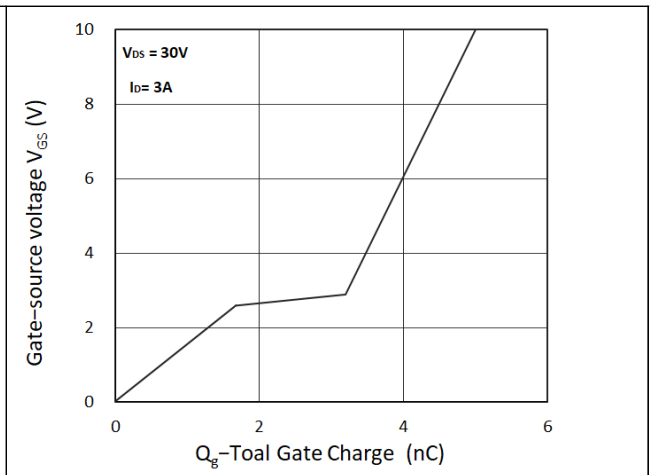


Figure 8. Gate Charge Characteristics

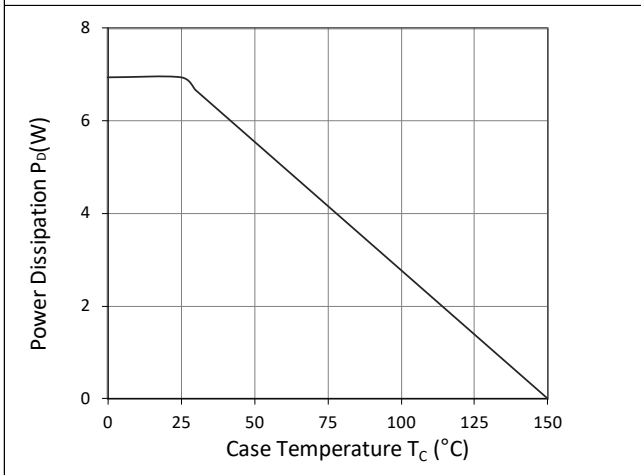


Figure 9. Power Dissipation

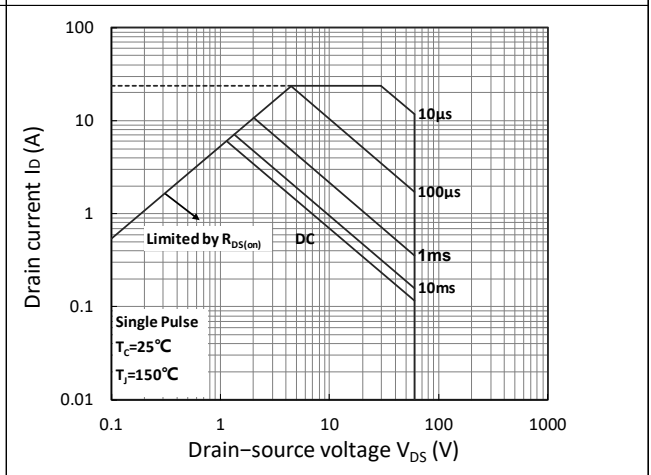


Figure 10. Safe Operating Area

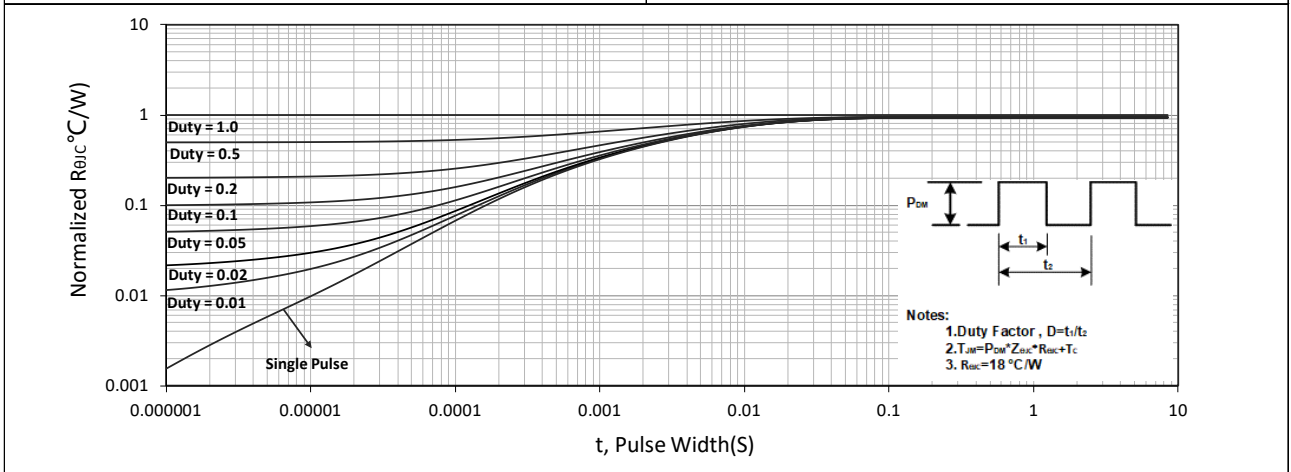


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

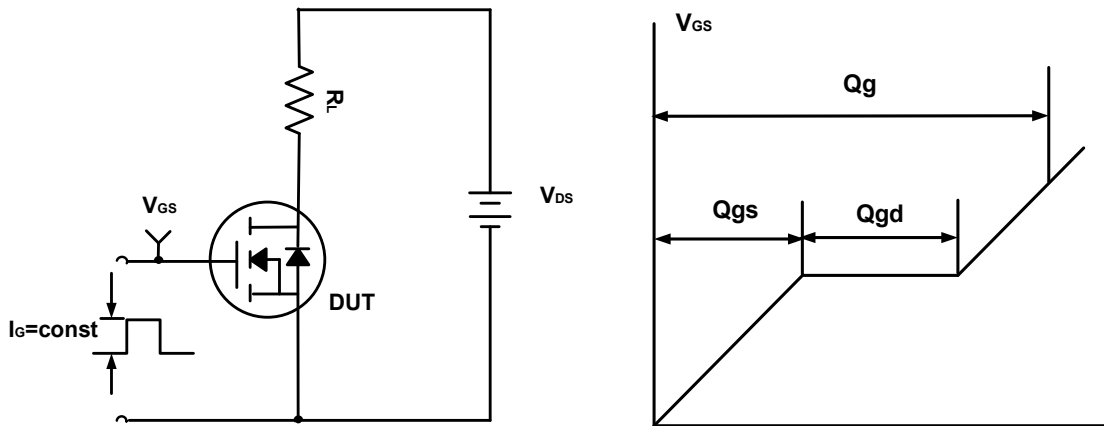


Figure A. Gate Charge Test Circuit & Waveforms

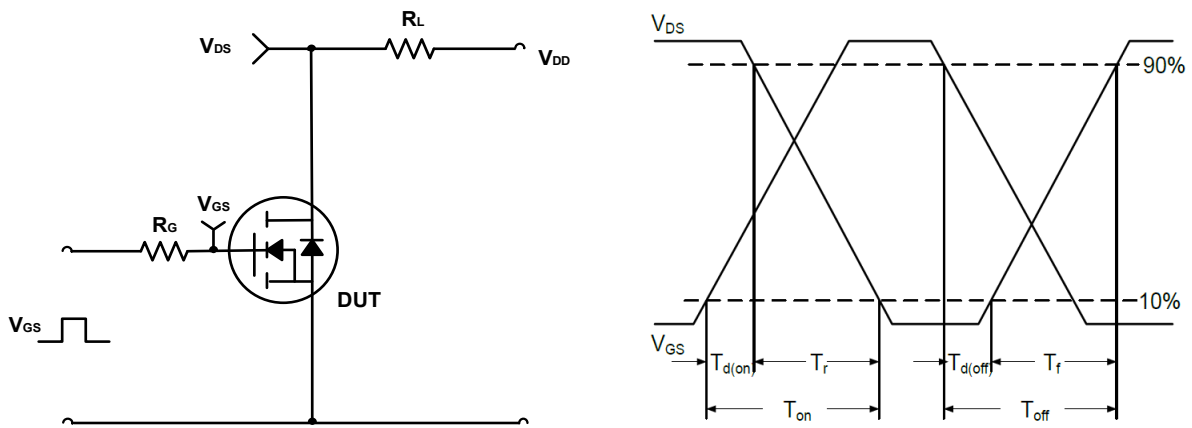


Figure B. Switching Test Circuit & Waveforms

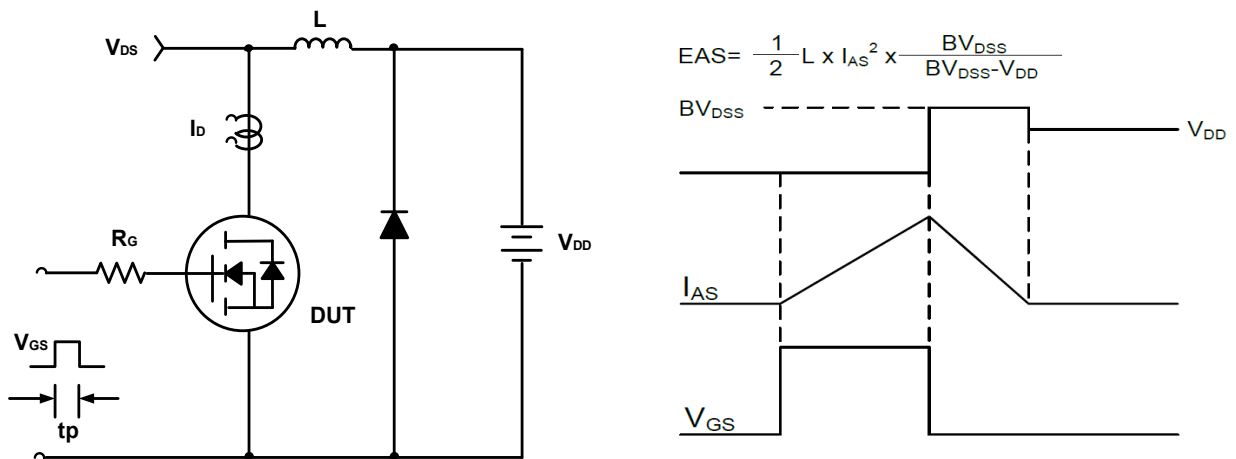
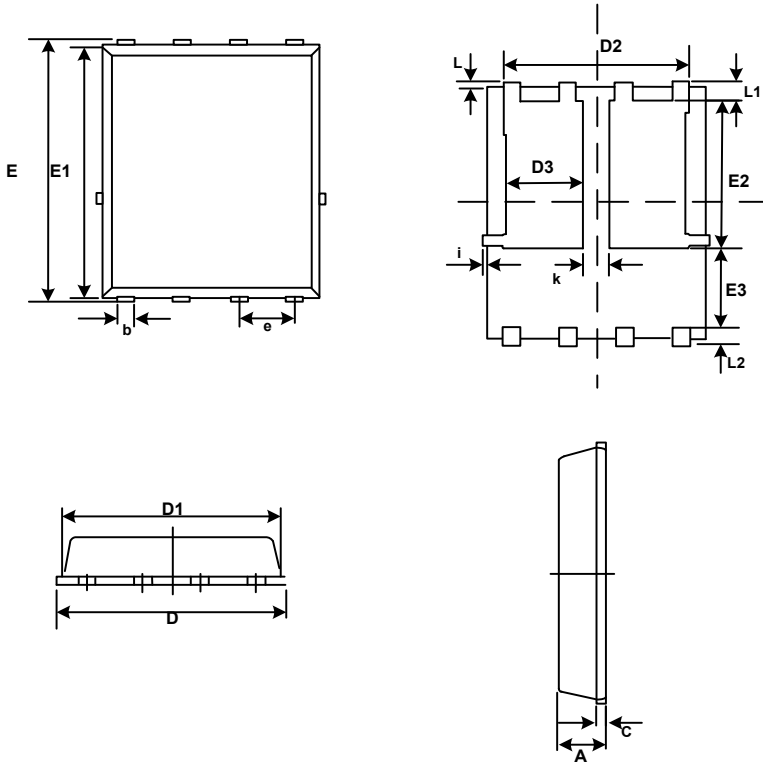


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Mechanical Dimensions for Dual PDFN5060D-8L

COMMON DIMENSIONS

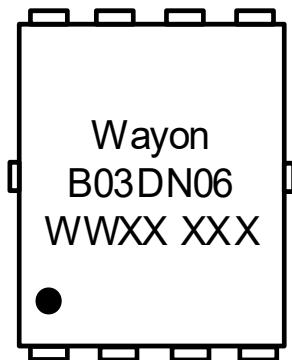


SYMBOL	MM	
	MIN	MAX
A	0.90	1.17
b	0.33	0.51
c	0.20BSC	
D	4.80	5.40
D1	4.80	5.00
D2	3.95	4.45
D3	1.55	1.80
E	5.90	6.15
E1	5.65	5.85
E2	3.30	3.78
E3	1.10	/
e	1.27BSC	
L	0.05	0.25
L1	0.38	0.61
L2	0.38	0.71
i	/	0.18
k	0.50	0.70

## Ordering Information

Part	Package	Marking	Packing method
WMB03DN06T1	PDFN5060D-8L	B03DN06	Tape and Reel

## Marking Information



B03DN06 = Device code

WWXX XXX= Date code

## Contact Information

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