

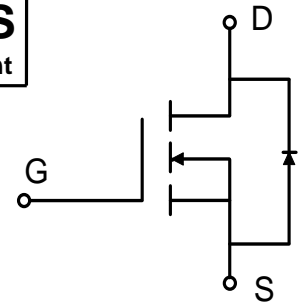
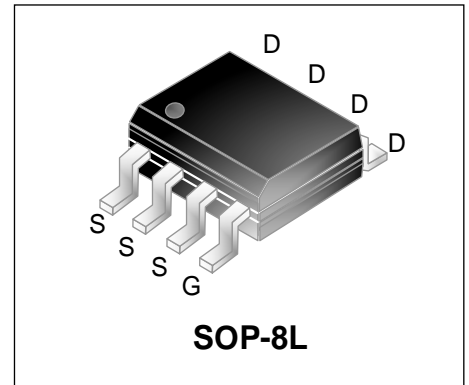
## 100V N-Channel Enhancement Mode Power MOSFET

### Description

WMS04N10T1 uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Features

- $V_{DS} = 100V$ ,  $I_D = 4A$   
 $R_{DS(on)} < 100m\Omega @ V_{GS} = 10V$   
 $R_{DS(on)} < 110m\Omega @ V_{GS} = 4.5V$
- Green Device Available
- Low Gate Charge
- Advanced High Cell Density Trench Technology
- 100% EAS Guaranteed



### Applications

- Power Management Switches
- DC/DC Converters

### Absolute Maximum Ratings (T<sub>A</sub> = 25°C, unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	T <sub>A</sub> =25°C	4
		T <sub>A</sub> =100°C	2.5
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	16	A
Single Pulse Avalanche Energy <sup>2</sup>	<b>EAS</b>	3.2	mJ
Total Power Dissipation	$P_D$	3.1	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	40.3	°C/W

**Electrical Characteristics** ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Static Characteristics</b>							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V	
Gate-Body Leakage Current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$T_J=25^\circ\text{C}$	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
	$T_J=100^\circ\text{C}$			-	-	100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	2	3	V	
Drain-Source on-Resistance <sup>4</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 4A$	-	68	100	m $\Omega$	
		$V_{GS} = 4.5V, I_D = 2A$	-	78	110		
Forward Transconductance <sup>4</sup>	$g_{fs}$	$V_{DS}=10V, I_D=4A$	-	11	-	S	
<b>Dynamic Characteristics<sup>5</sup></b>							
Input Capacitance	$C_{iss}$	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1\text{MHz}$	-	1233	-	$\mu F$	
Output Capacitance	$C_{oss}$		-	32	-		
Reverse Transfer Capacitance	$C_{rss}$		-	26	-		
Gate Resistance	$R_g$	$f = 1\text{MHz}$	-	1.4	-	$\Omega$	
<b>Switching Characteristics<sup>5</sup></b>							
Total Gate Charge	$Q_g$	$V_{GS} = 10V, V_{DS} = 50V,$ $I_D=4A$	-	12	-	nC	
Gate-Source Charge	$Q_{gs}$		-	2.9	-		
Gate-Drain Charge	$Q_{gd}$		-	1.8	-		
Turn-on Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 50V,$ $R_G = 3\Omega, I_D = 4A$	-	3.9	-	ns	
Rise Time	$t_r$		-	26	-		
Turn-off Delay Time	$t_{d(off)}$		-	16.2	-		
Fall Time	$t_f$		-	8.9	-		
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 4A, di/dt=100A/\mu s$	-	40	-	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	43	-	nC	
<b>Drain-Source Body Diode Characteristics</b>							
Diode Forward Voltage <sup>4</sup>	$V_{SD}$	$I_S = 1A, V_{GS} = 0V$	-	-	1.2	V	
Continuous Source Current	$I_S$	$T_A=25^\circ\text{C}$	-	-	4	A	

## Notes:

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ .
2. The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}= 8A$  .
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$ .
5. This value is guaranteed by design hence it is not included in the production test..

Typical Characteristics

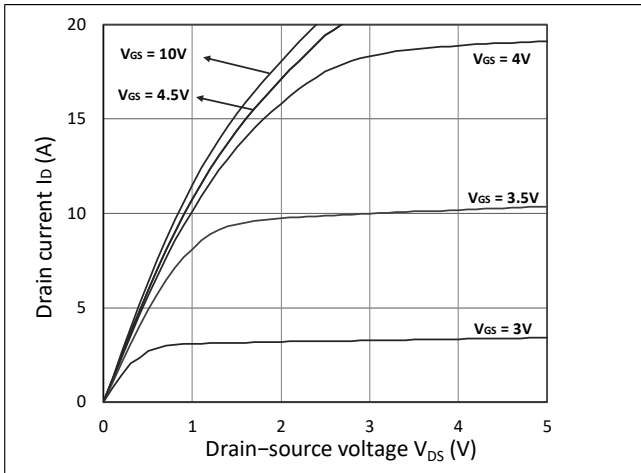


Figure 1. Output Characteristics

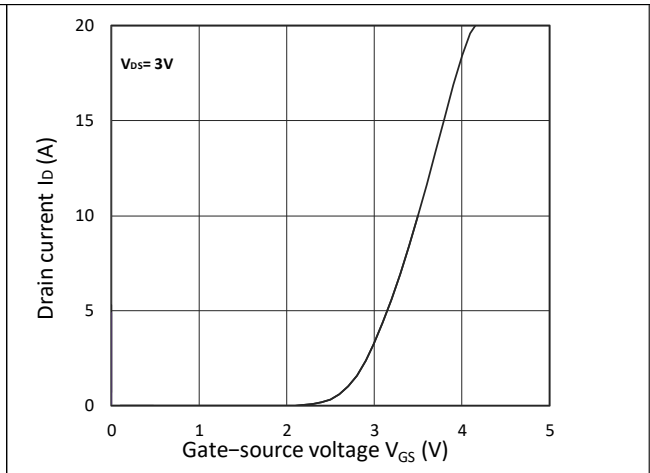


Figure 2. Transfer Characteristics

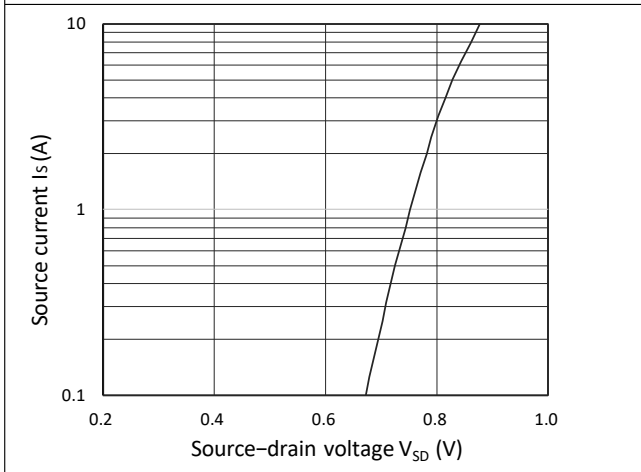


Figure 3. Forward Characteristics of Reverse

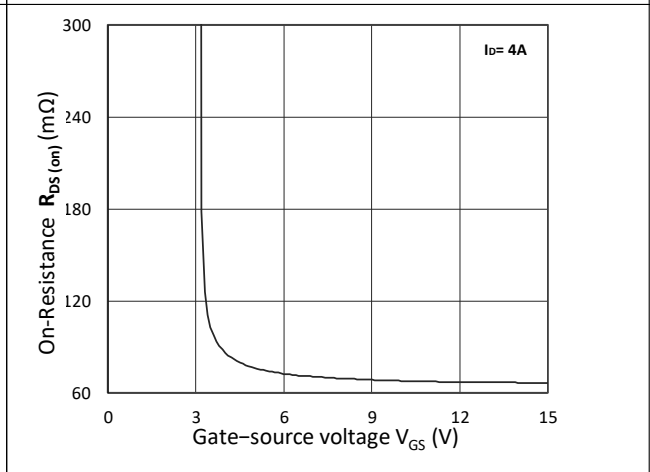


Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$

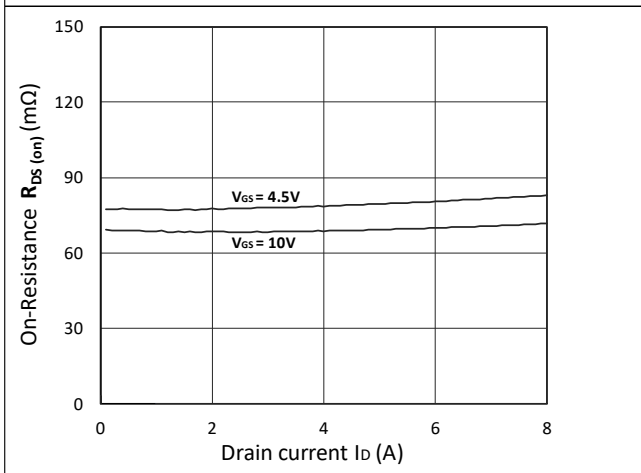


Figure 5.  $R_{DS(ON)}$  vs.  $I_D$

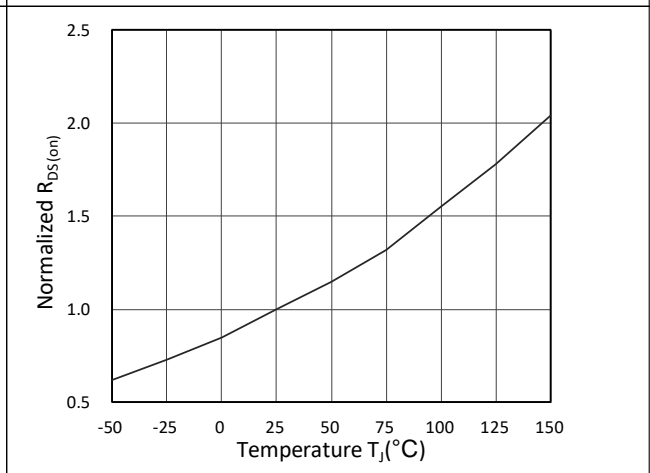


Figure 6. Normalized  $R_{DS(ON)}$  vs. Temperature

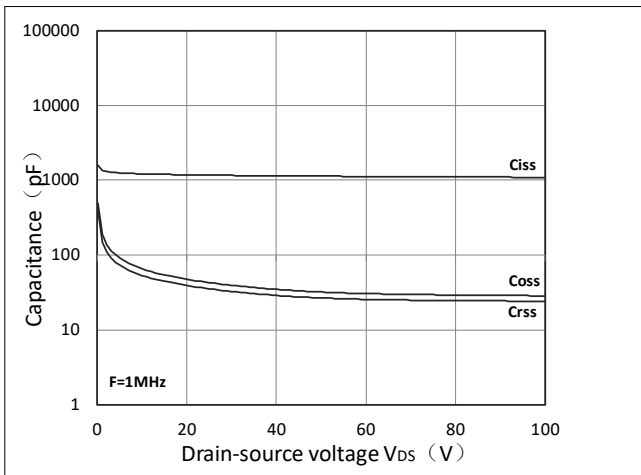


Figure 7. Capacitance Characteristics

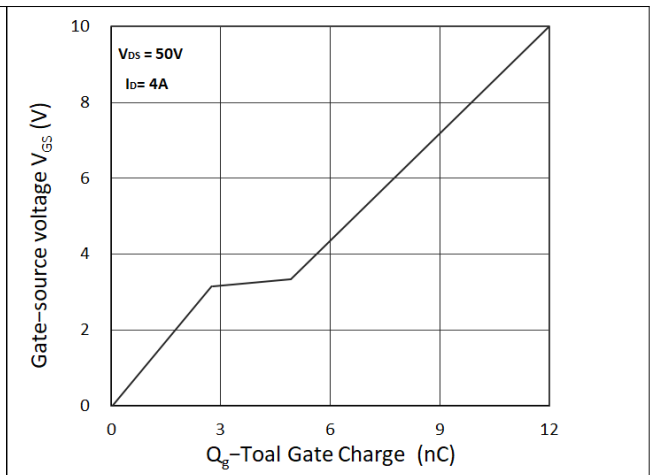


Figure 8. Gate Charge Characteristics

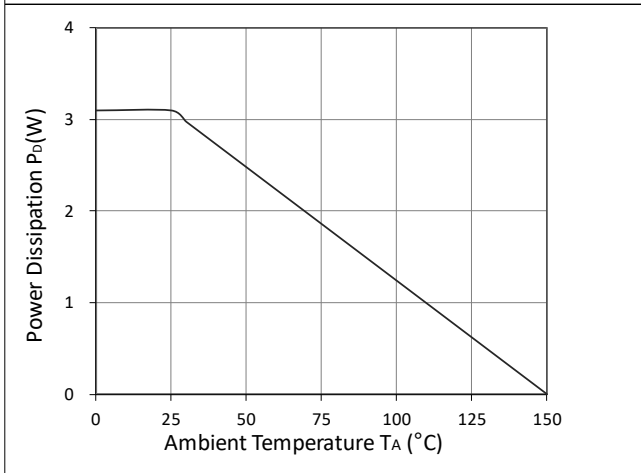


Figure 9. Power Dissipation

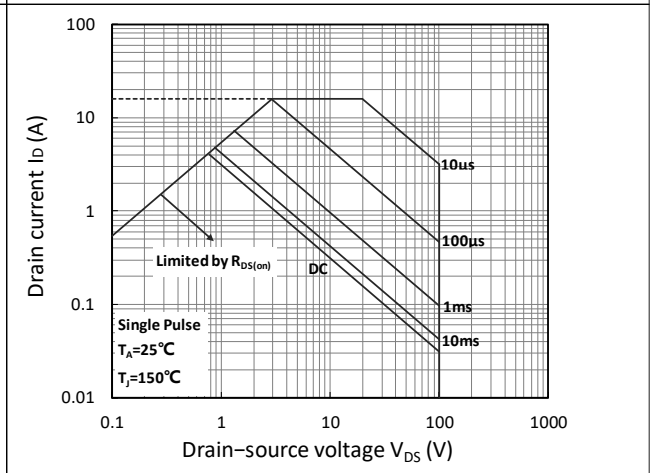


Figure 10. Safe Operating Area

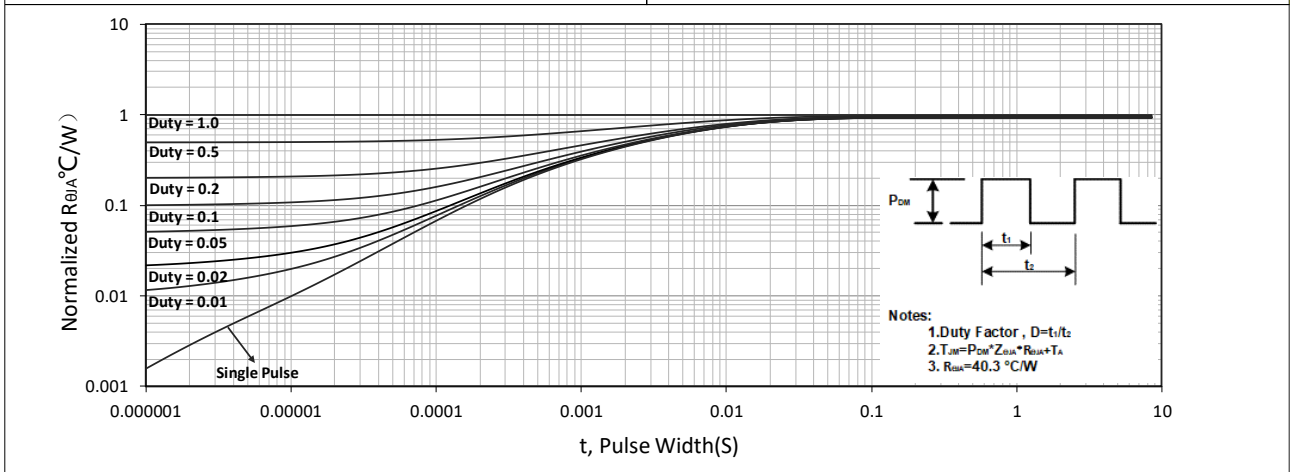


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

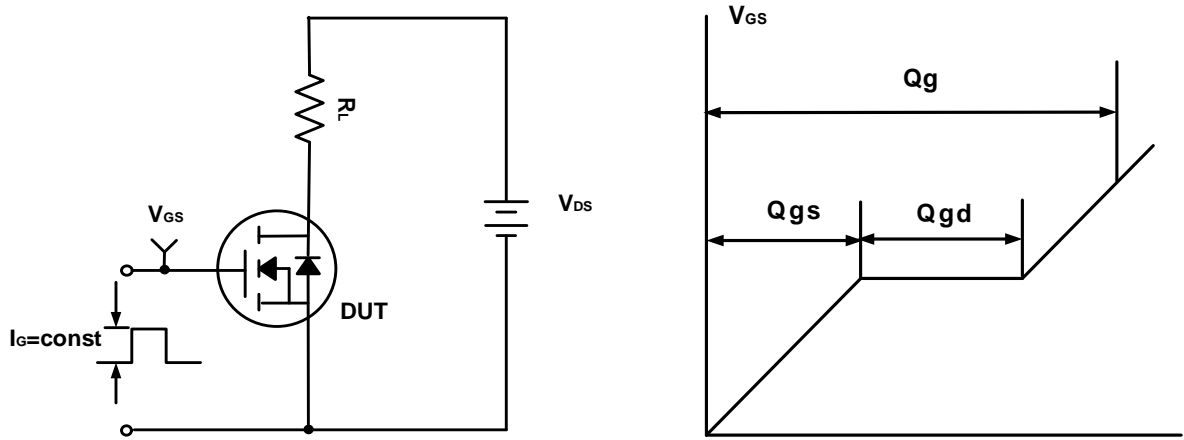


Figure A. Gate Charge Test Circuit & Waveforms

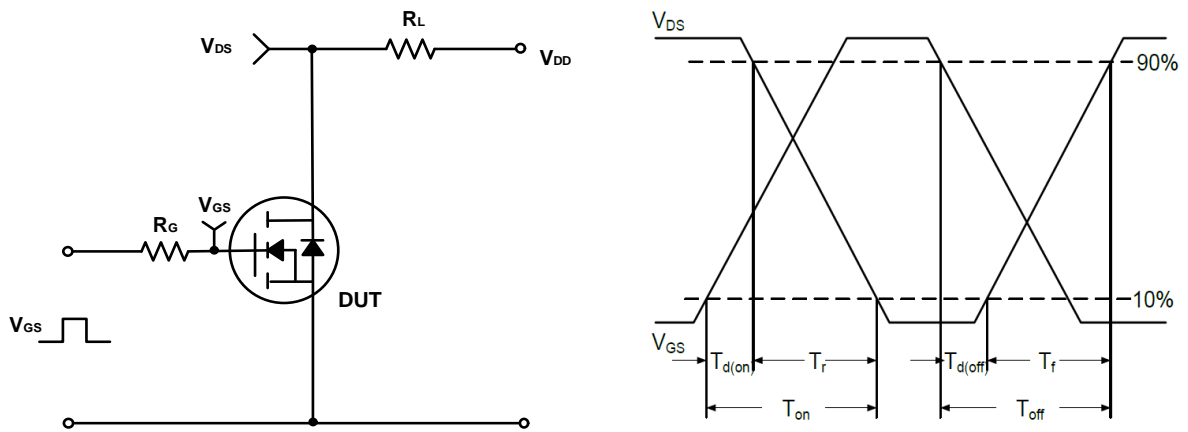


Figure B. Switching Test Circuit & Waveforms

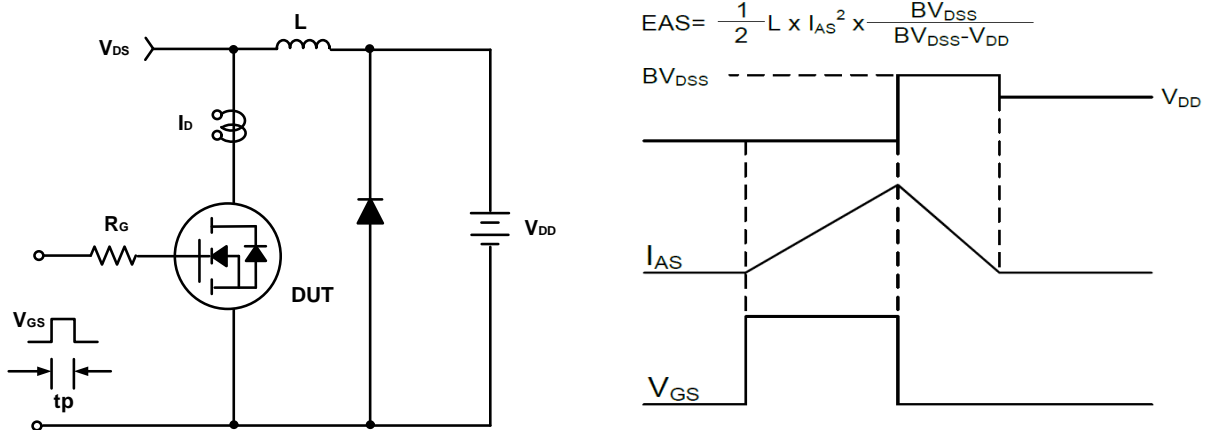
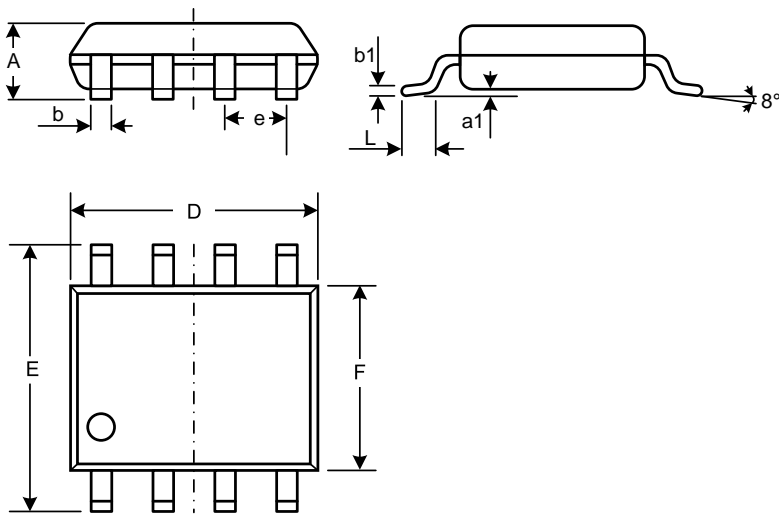


Figure C. Unclamped Inductive Switching Circuit & Waveforms

## Mechanical Dimensions for SOP-8L



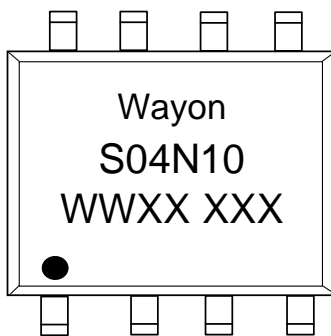
## COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	1.35	1.75
a1	0.05	0.25
b	0.31	0.51
b1	0.16	0.25
D	4.70	5.15
E	5.75	6.25
e	1.07	1.47
F	3.70	4.10
L	0.40	1.27

## Ordering Information

Part	Package	Marking	Packing method
WMS04N10T1	SOP-8L	S04N10	Tape and Reel

## Marking Information



S04N10 = Device code

WWXX XXX= Date code

## Contact Information

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